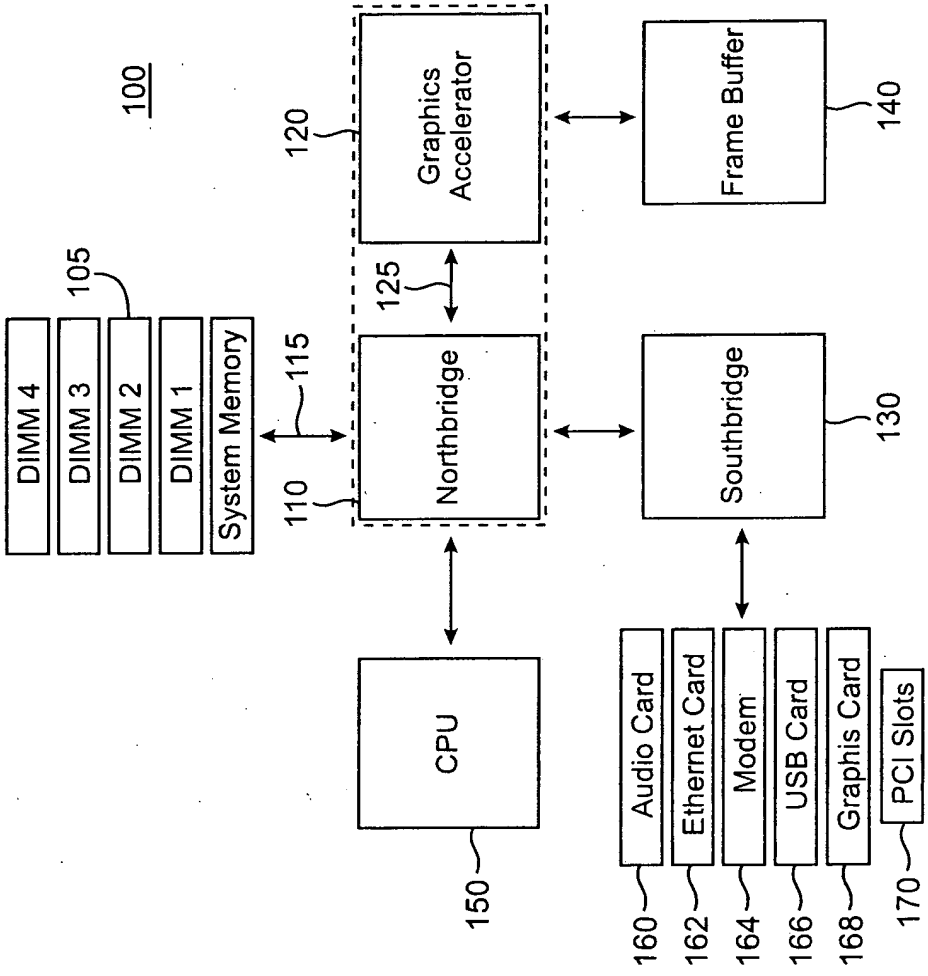


FIG. 1

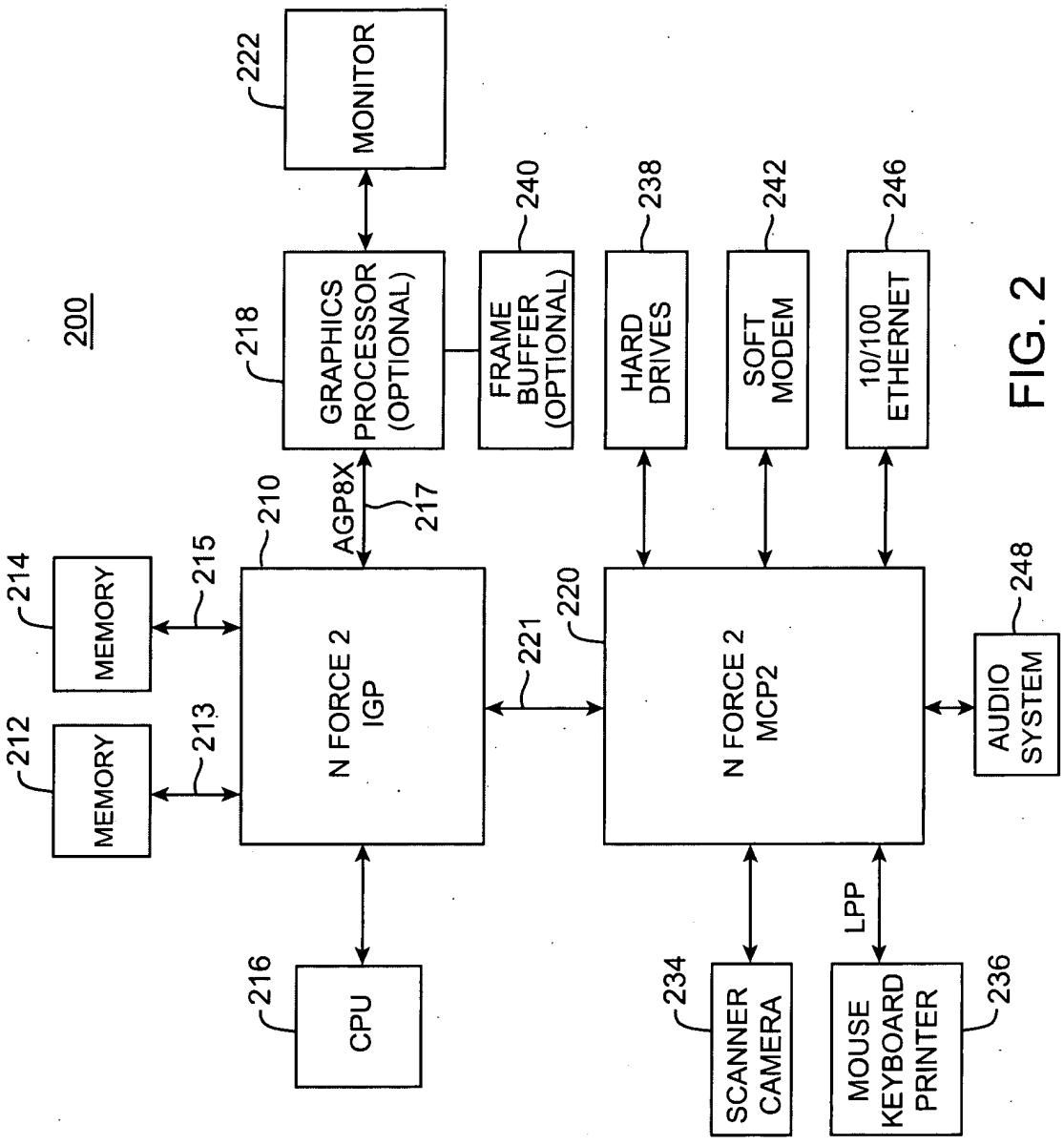
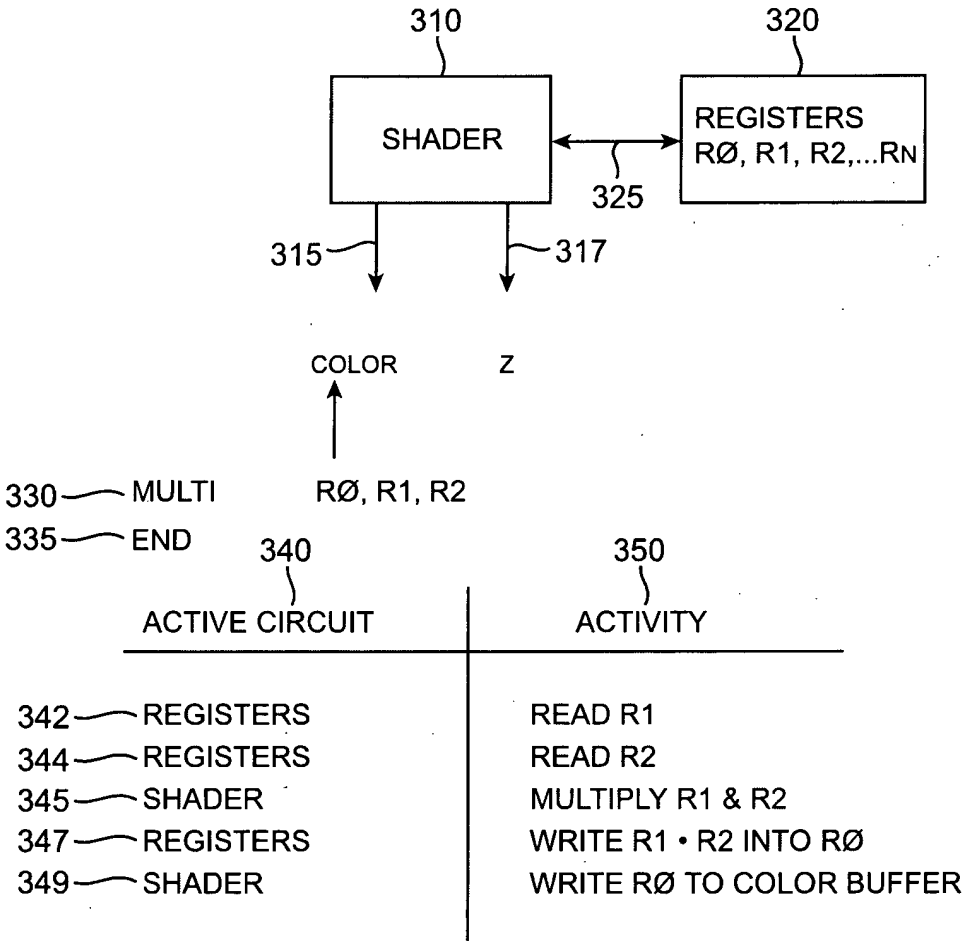
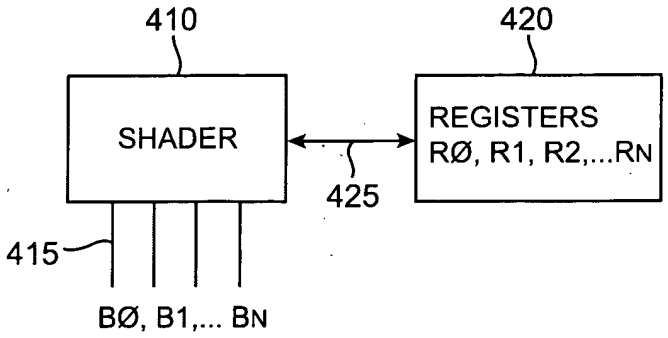


FIG. 2



PRIOR ART

FIG. 3



430 MULTI RØ, R1, R2
440 ADD R1, RØ, R1
450 END

MORE BUFFERS =
MORE STEPS PER PASS +
FEWER PASSES

	460 ACTIVE CIRCUIT	470 ACTIVITY
462	REGISTERS	READ R1
464	REGISTERS	READ R2
466	SHADER	MULTIPLY R1 & R2
468	REGISTERS	WRITE R1 • R2 INTO RØ
472	REGISTERS	READ RØ
474	REGISTERS	READ R1
476	SHADER	ADD RØ & R1
478	REGISTERS	WRITE RØ + R1 INTO R1
482	SHADER	WRITE RØ AND R1 INTO BUFFERS

FIG. 4

```
510 — MULTI RØ , R1, R2

520 — PST RØ , #ZL

530 — ADD RØ , R3 , R4

540 — PLD R1 , #ZH
```

```
550 — PLD RØ , #id          INDIRECT (FIXED)

552 — PLD RØ , @ R1         IDENTIFICATION (MOVABLE)

554 — PLD RØ , # address    DIRECT REFERENCE

556 — PLD RØ , @ R1         ADDRESS
```

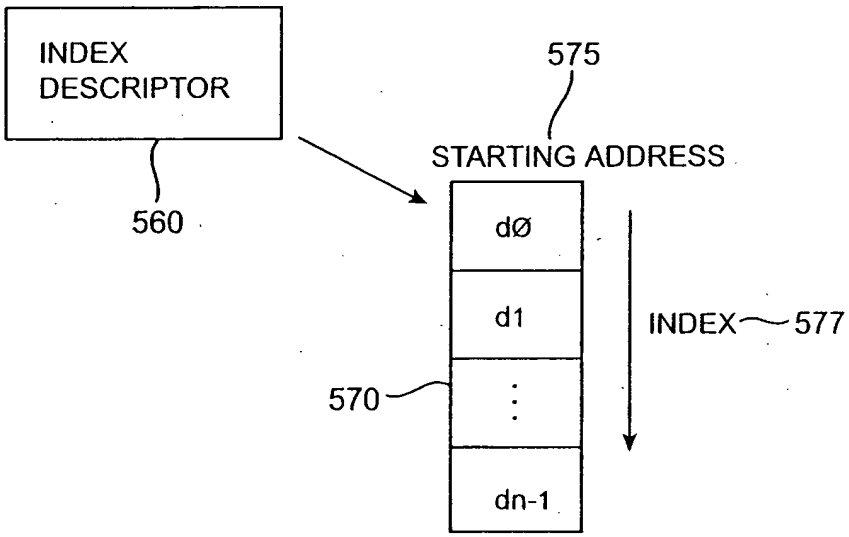
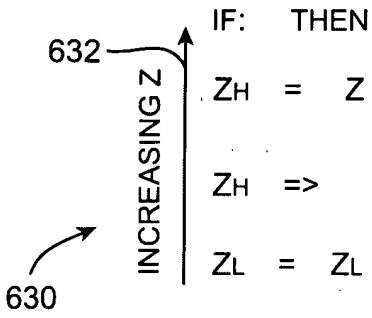
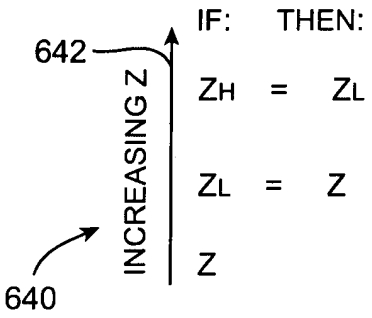


FIG. 5

610 IF (Z_L < Z AND Z < Z_H) SET Z_H = Z

620 IF (Z <= Z_L) SET Z_H = Z_L , SET Z_L = Z





650 COMMANDS	670 RØ	672 R1	674 R2	676 R3	678 ZH	679 ZL
652 PLD RØ , #ZL	ZL	-	-	-	ZH	ZL
654 PLD R1 , #ZH	ZL	ZH	-	-	ZH	ZL
656 LT R2 , RØ , Z	ZL	ZH	FALSE	-	ZH	ZL
658 LT R3 , Z , R1	ZL	ZH	FALSE	TRUE	ZH	ZL
660 AND R3 , R2 , R3	ZL	ZH	FALSE	FALSE	ZH	ZL
662 PSTC #ZH , Z , R3	ZL	ZH	FALSE	FALSE	ZH	ZL
664 PSTC #ZL , Z ,~ R2	ZL	ZH	FALSE	FALSE	ZH	Z
665 PSTC #ZH , RØ ,~ R2	ZL	ZH	FALSE	FALSE	ZL	Z

FIG. 6

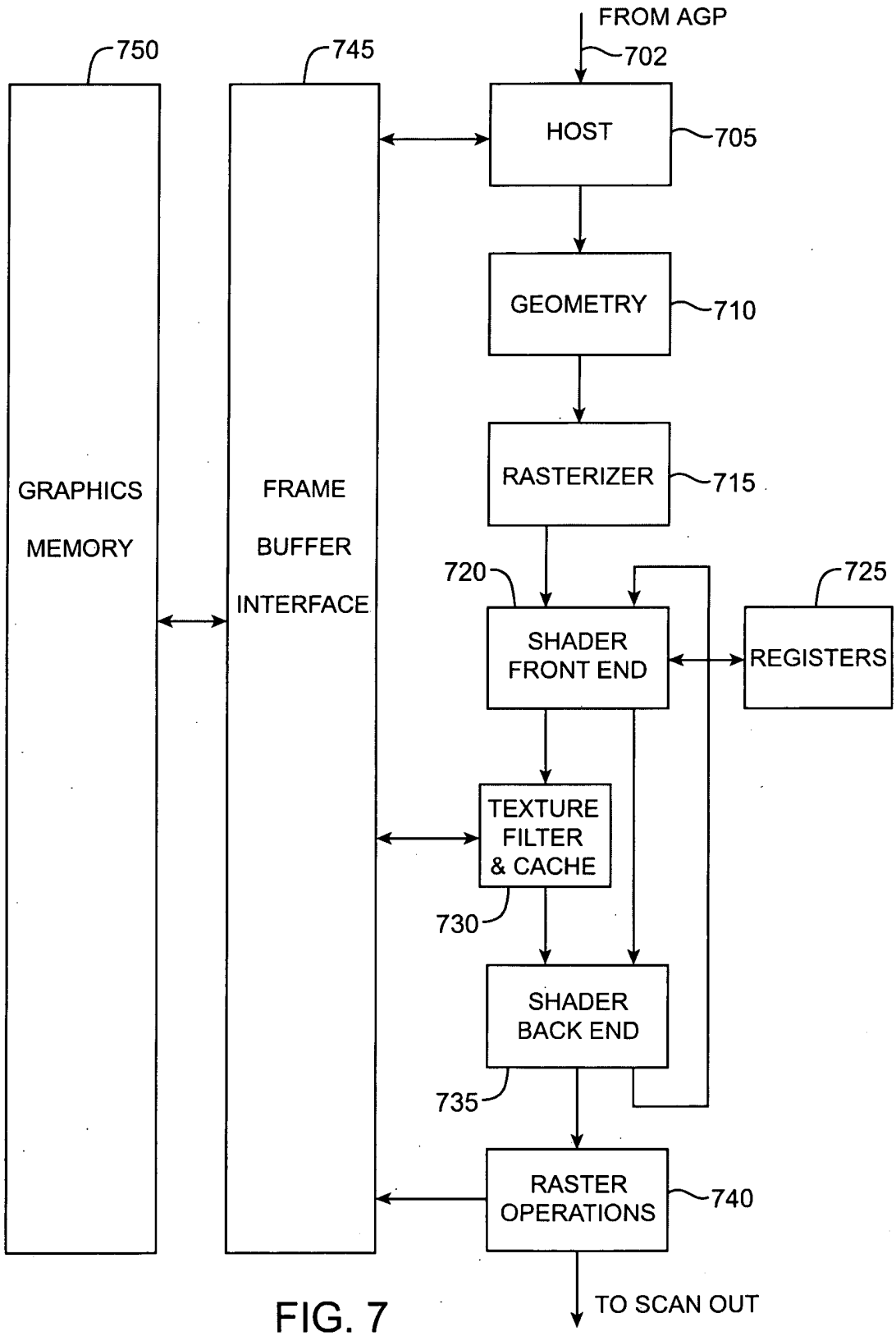

FROM AGP
702
750
745
HOST
705
GEOMETRY
710
RASTERIZER
715
GRAPHICS MEMORY
FRAME BUFFER INTERFACE
720
725
SHADER FRONT END
REGISTERS
TEXTURE FILTER & CACHE
730
SHADER BACK END
735
RASTER OPERATIONS
740
TO SCAN OUT

FIG. 7